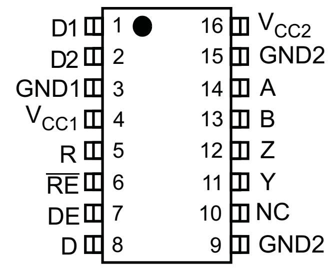
# Isolated 3.3V RS-485 Transceiver With Integrated Transformer Driver

**Check for Samples: ISO35T**

## FEATURES

- **3000$V_{RMS}$ / 4242$V_{PK}$ Isolation**
- **Bus-Pin ESD Protection**
  - **16 kV HBM Between Bus-Pins and GND2**
  - **6 kV HBM Between Bus-Pins and GND1**
- **1/8 Unit Load – Up to 256 Nodes on a Bus**
- **Designed for RS-485 and RS-422 Applications**
- **Signaling Rates up to 1 Mbps**
- **Thermal Shutdown Protection**
- **Typical Efficiency > 60% ($I_{LOAD}$ = 100 mA) - see *sluu470***
- **Low Driver Bus Capacitance 16 pF (Typ)**
- **50 kV/μs Typical Transient Immunity**
- **UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2) Approvals Pending**
- **Fail-safe Receiver for Bus Open, Short, Idle**
- **Logic Inputs are 5-V Tolerant**

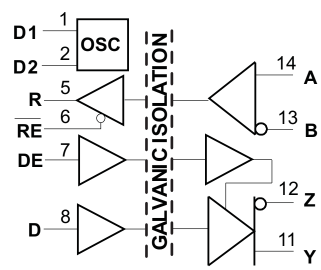
**DW PACKAGE**




## APPLICATIONS

- **Isolated RS-485/RS-422 Interfaces**
- **Factory Automation**
- **Motor/Motion Control**
- **HVAC and Building Automation Networks**
- **Networked Security Stations**

## FUNCTION DIAGRAM



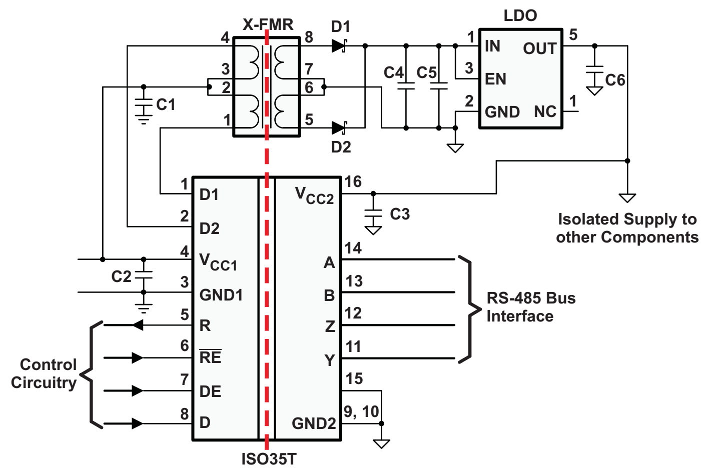

## DESCRIPTION

The ISO35T is an isolated differential line transceiver with integrated oscillator outputs that provide the primary voltage for an isolation transformer. The device is a full-duplex differential line transceiver for RS-485 and RS-422 applications that can easily be configured for half-duplex operation by connecting pin 11 to pin 14, and pin 12 to pin 13.

These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 4242$V_{PK}$ of isolation per VDE for 60s between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. The ISO35T can significantly reduce the risk of data corruption and damage to expensive control circuits.

The ISO35T is specified for use from –40°C to 85°C.




**Typical Application Circuit (For details see *sluu470*)**

## PIN DESCRIPTIONS

| NAME | PIN # | FUNCTION |
|---|---|---|
| D1 | 1 | Transformer Driver Terminal 1, Open Drain Output |
| D2 | 2 | Transformer Driver Terminal 2, Open Drain Output |
| GND1 | 3 | Logic-side Ground |
| $V_{CC1}$ | 4 | Logic-side Power Supply |
| R | 5 | Receiver Output |
| $\overline{RE}$ | 6 | Receiver Enable Input. This pin has complementary logic. |
| DE | 7 | Driver Enable Input |
| D | 8 | Driver Input |
| GND2 | 9, 15 | Bus-side Ground. Both pins are internally connected. |
| NC | 10 | No Connect. This pin is not connected to any internal circuitry. |
| Y | 11 | Non-inverting Driver Output |
| Z | 12 | Inverting Driver Output |
| B | 13 | Inverting Receiver Input |
| A | 14 | Non-inverting Receiver Input |
| $V_{CC2}$ | 16 | Bus-side Power Supply |

## ABSOLUTE MAXIMUM RATINGS(1)

| | | | | | VALUE | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$,$V_{CC2}$ | Input supply voltage(2) | | | | –0.3 to 6 | V |
| $V_A$,$V_B$,$V_Y$,$V_Z$ | Voltage at any bus I/O terminal (A, B, Y, Z) | | | | –9 to 14 | V |
| $V_{D1}$,$V_{D2}$ | Voltage at D1, D2 | | | | 14 | V |
| $V_{(TRANS)}$ | Voltage input, transient pulse through 100Ω, see Figure 12 (A,B,Y,Z) | | | | –50 to +50 | V |
| $V_I$ | Voltage input at any D, DE or $\overline{RE}$ terminal | | | | –0.5 to 7 | V |
| $I_O$ | Receiver output current | | | | ±10 | mA |
| $I_{D1}$,$I_{D2}$ | Transformer Driver Output Current | | | | 450 | mA |
| ESD | Electrostatic discharge | Human Body Model | JEDEC Standard 22, Test Method A114-C.01 | Bus pins and GND1 | ±6 | kV |
| | | | | Bus pins and GND2 | ±16 | kV |
| | | | | All pins | ±4 | kV |
| | | Charged Device Model | JEDEC Standard 22, Test Method C101 | All pins | ±1.5 | kV |
| | | Machine Model | ANSI/ESDS5.2-1996 | | ±200 | V |
| $T_J$ | Maximum junction temperature | | | | 170 | °C |
| $T_{STG}$ | Storage temperature | | | | -65 to 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$,$V_{CC2}$ | Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common-mode) | | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage | D, DE, $\overline{RE}$ | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | D, DE, $\overline{RE}$ | 0 | | 0.8 | V |
| $V_{ID}$ | Differential input voltage | A with respect to B | –12 | | 12 | V |
| $R_L$ | Differential load resistance | | 54 | 60 | | Ω |
| $I_O$ | Output Current | Driver | –60 | | 60 | mA |
| | | Receiver | –8 | | 8 | mA |
| $T_A$ | Ambient temperature | | -40 | | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 150 | °C |
| 1 / $t_{UI}$ | Signaling Rate | | | | 1 | Mbps |

## SUPPLY CURRENT & COMMON MODE TRANSIENT IMMUNITY

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC1}$(1) | Logic-side quiescent supply current | DE & $\overline{RE}$ = 0V or $V_{CC1}$ (Driver and Receiver Enabled or Disabled), D = 0 V or $V_{CC1}$, No load | | 4.5 | 8 | mA |
| $I_{CC2}$(1) | Bus-side quiescent supply current | $\overline{RE}$ = 0 V or $V_{CC1}$, DE = 0 V (driver disabled), No load | | 7.5 | 13 | mA |
| | | $\overline{RE}$ = 0 V or $V_{CC1}$, DE = $V_{CC1}$ (driver enabled), D = 0 V or $V_{CC1}$, No Load | | 9 | 16 | |
| CMTI | Common-mode transient immunity | See Figure 13 | 25 | 50 | | kV/μs |

(1) $I_{CC1}$ and $I_{CC2}$ are measured when device is connected to external power supplies, $V_{CC1}$ & $V_{CC2}$. In this case, D1 & D2 are open and disconnected from external transformer.

## RS-485 DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\|V_{OD}\|$ | Differential output voltage magnitude | $I_O$ = 0 mA (No Load) | | 2.5 | | $V_{CC2}$ | V |
| | | $R_L$ = 54 Ω (RS-485), See Figure 1 | | 1.5 | 2 | | |
| | | $R_L$ = 100 Ω (RS-422)(1), See Figure 1 | | 2 | 2.3 | | |
| | | $V_{test}$ = –7 V to +12 V, See Figure 2 | | 1.5 | | | |
| $\Delta\|V_{OD}\|$ | Change in magnitude of the differential output voltage | See Figure 1 and Figure 2 | | –0.2 | 0 | 0.2 | V |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | Figure 3 | | 1 | 2.6 | 3 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage | | | –0.1 | | 0.1 | V |
| $V_{OC(pp)}$ | Peak-to-peak common-mode output voltage | See Figure 3 | | | 0.25 | | V |
| $I_I$ | Input current, D & DE | $V_I$ at 0 V or $V_{CC1}$ | | –10 | | 10 | μA |
| $I_{OZ}$ | High-impedance state output current | $V_Y$ or $V_Z$ = 12V, $V_{CC}$ = 0 V or 3 V, DE = 0 V | Other input at 0 V | | | 90 | μA |
| | | $V_Y$ or $V_Z$ = –7 V, $V_{CC}$ = 0 V or 3 V, DE = 0 V | | –10 | | | |
| $I_{OS(P)}$ (2) | Peak short-circuit output current | $V_Y$ or $V_Z$ = –7 V to +12 V, See Figure 4 | Other input at 0 V | | 300 | | mA |
| $I_{OS(SS)}$ (2) | Steady-state short-circuit output current | | | -250 | | 250 | mA |
| $C_{(OD)}$ | Differential output capacitance | $V_I$ = 0.4 sin (4E6πt) + 0.5V, DE at 0 V | | | 16 | | pF |

(1) $V_{CC2}$ = 3.3 V ± 5%
(2) This device has thermal shutdown and output current-limiting features to protect in short-circuit fault condition.

## RS-485 DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | See Figure 5 | | 205 | 340 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} – t_{PLH}\|$) | | | 1.5 | | |
| $t_r$ | Differential output signal rise time | | 120 | 185 | 300 | |
| $t_f$ | Differential output signal fall time | | 120 | 180 | 300 | |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | See Figure 6 | | | 205 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | | | 530 | |
| $t_{PLZ}$ | Propagation delay, low-level to high-impedance output | See Figure 7 | | | 330 | |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | | | 530 | |

## RS-485 RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT(+)}$ | Positive-going input threshold voltage | $I_O$ = -8 mA | | | | –20 | mV |
| $V_{IT(–)}$ | Negative-going input threshold voltage | $I_O$ = 8 mA | | –200 | | | |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+}$ – $V_{IT–}$) | | | | 50 | | mV |
| $V_{OH}$ | High-level output voltage | See Figure 8 | $V_{ID}$ = +200 mV, $I_O$ = -8 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{ID}$ = –200 mV, $I_O$ = 8 mA | | | 0.4 | |
| $I_{O(Z)}$ | High-impedance state output current | $V_O$ = 0 or $V_{CC1}$, $\overline{RE}$ = $V_{CC1}$ | | –1 | | 1 | μA |

## RS-485 RECEIVER ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_A$, $I_B$ | Bus input current | $V_A$ or $V_B$ = 12 V | Other input at 0 V | | 50 | 100 | μA |
| | | $V_A$ or $V_B$ = 12 V, $V_{CC2}$ = 0 V | | | 60 | 100 | |
| | | $V_A$ or $V_B$ = –7 V | | –100 | –40 | | |
| | | $V_A$ or $V_B$ = -7 V, $V_{CC2}$ = 0 V | | –100 | –30 | | |
| $I_{IH}$ | High-level input current, $\overline{RE}$ | $V_{IH}$ = 2. V | | –10 | | 10 | μA |
| $I_{IL}$ | Low-level input current, $\overline{RE}$ | VIL = 0.8 V | | –10 | | 10 | |
| $R_{ID}$ | Differential input resistance | Measured between A & B | | 96 | | | kΩ |
| $C_{ID}$ | Differential input capacitance | $V_I$ = 0.4 sin (4E6πt) + 0.5V, DE at 0 V | | | 2 | | pF |

## RS-485 RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | See Figure 9 | | 85 | 115 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} – t_{PLH}\|$) | | | | 13 | |
| $t_r$ | Output signal rise time | | | 1 | 4 | |
| $t_f$ | Output signal fall time | | | 1 | 4 | |
| $t_{PHZ}$, $t_{PZH}$ | Propagation delay, high-level to high-impedance output<br>Propagation delay, high-impedance to high-level output | See Figure 10, DE at 0 V | | 13 | 25 | ns |
| $t_{PLZ}$ $t_{PZL}$ | Propagation delay, low-level to high-impedance output<br>Propagation delay, high-impedance to low-level output | See Figure 11, DE at 0 V | | 13 | 25 | |

## TRANSFORMER DRIVER CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | Oscillator frequency | $V_{CC1}$ = 3.3V ± 10%, D1 and D2 connected to Transformer | 300 | 400 | 550 | kHz |
| $R_{ON}$ | Switch on resistance | D1 and D2 connected to 50Ω pull-up resistors | | 1 | 2.5 | Ω |
| $t_{r\_D}$ | D1, D2 output rise time | $V_{CC1}$ = 3.3V ± 10%, see Figure 14 | 30 | 70 | 110 | ns |
| $t_{f\_D}$ | D1, D2 output fall time | $V_{CC1}$ = 3.3V ± 10%, see Figure 14 | 40 | 80 | 140 | ns |
| $f_{St}$ | Startup frequency | $V_{CC1}$ = 1.9 V, D1 and D2 connected to Transformer | | 230 | | kHz |
| $t_{BBM}$ | Break before make time delay | $V_{CC1}$ = 3.3V ± 10%, see Figure 14 | 100 | 140 | 200 | ns |

## PARAMETER MEASUREMENT INFORMATION

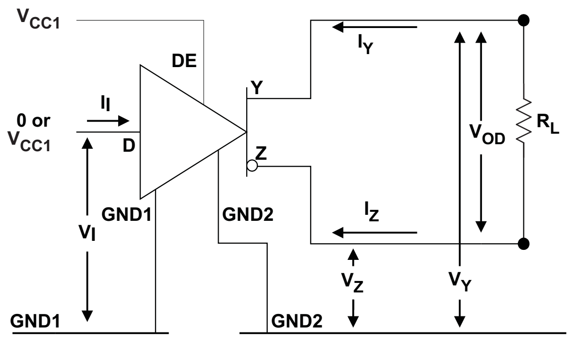


Figure 1. Driver $V_{OD}$ Test and Current Definitions

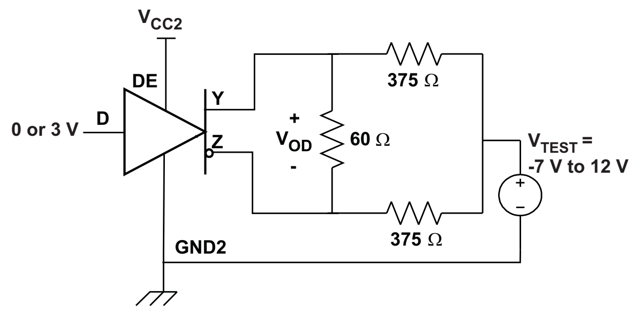


Figure 2. Driver $V_{OD}$ With Common-Mode Loading Test Circuit

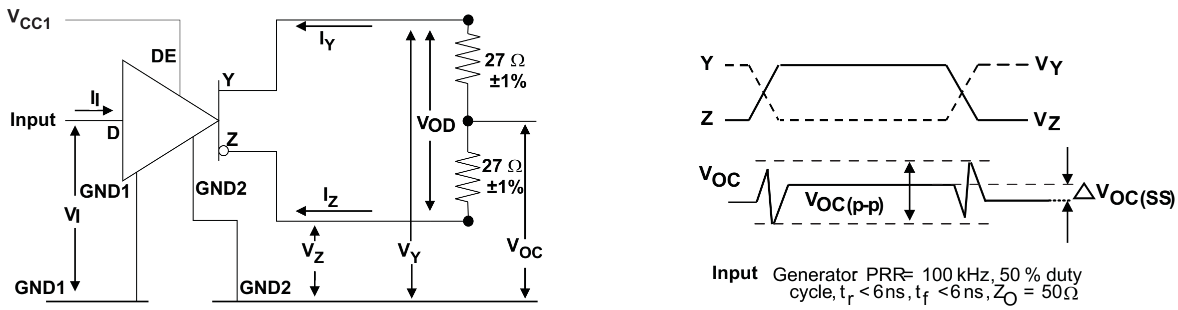


Figure 3. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

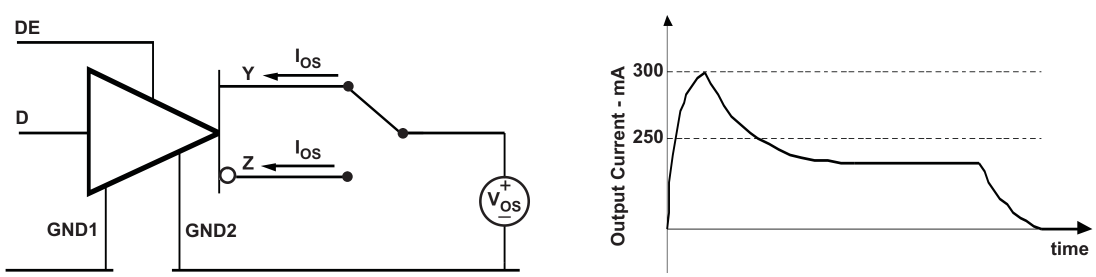


Figure 4. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0

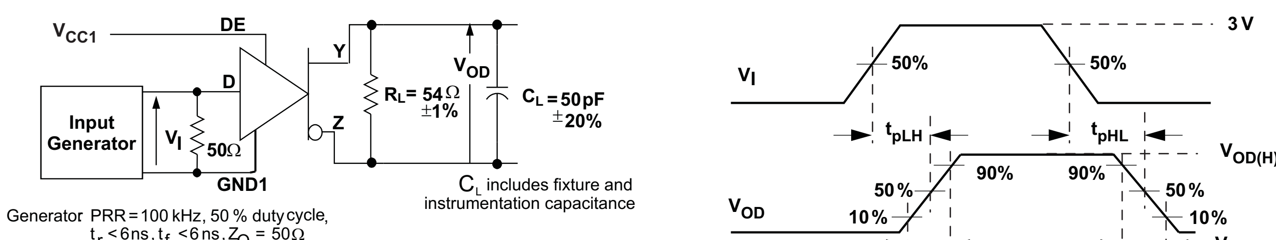


Figure 5. Driver Switching Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION (continued)

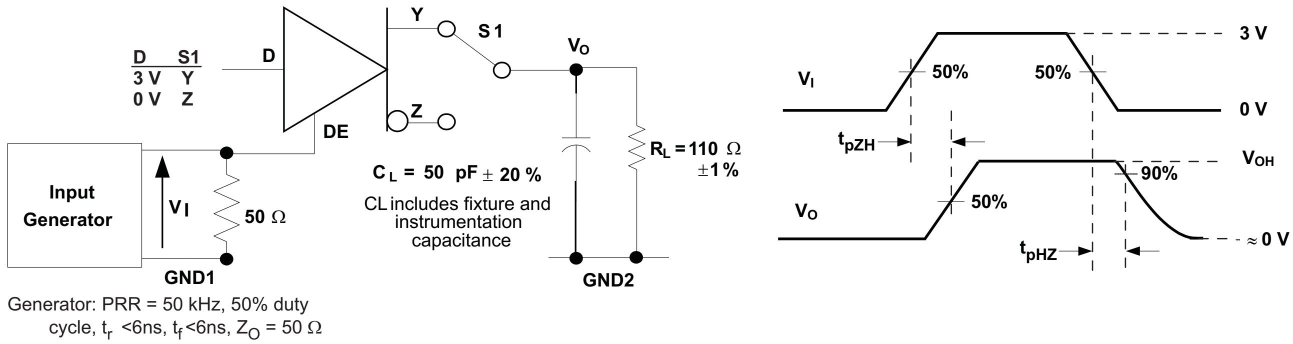



Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

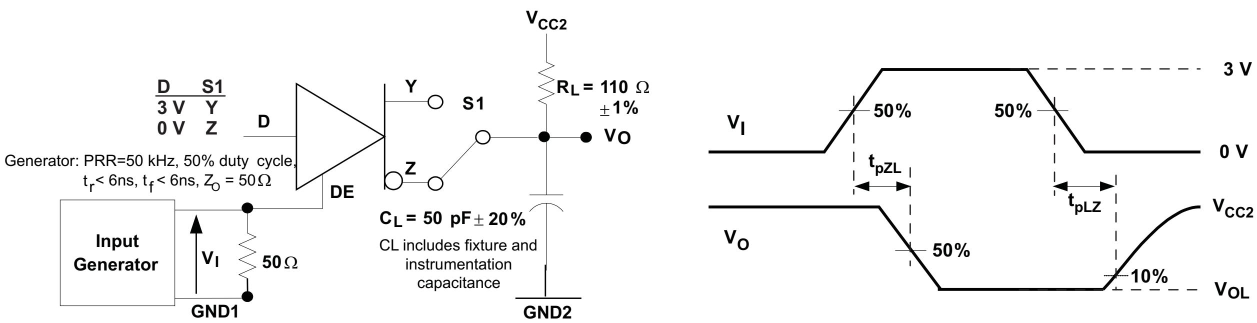



Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

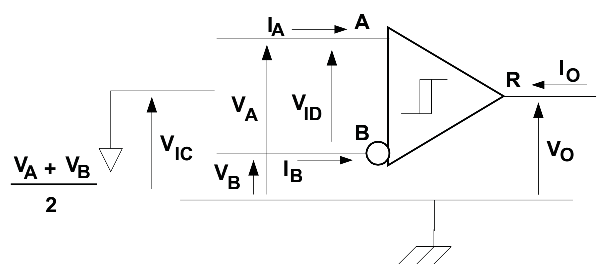



Figure 8. Receiver Voltage and Current Definitions

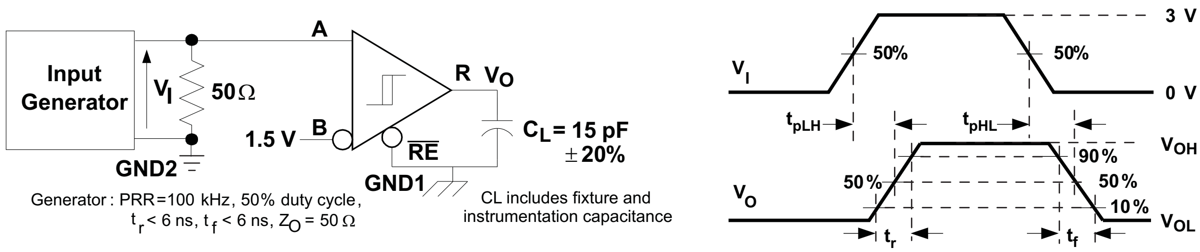



Figure 9. Receiver Switching Test Circuit and Waveforms

## PARAMETER MEASUREMENT INFORMATION (continued)

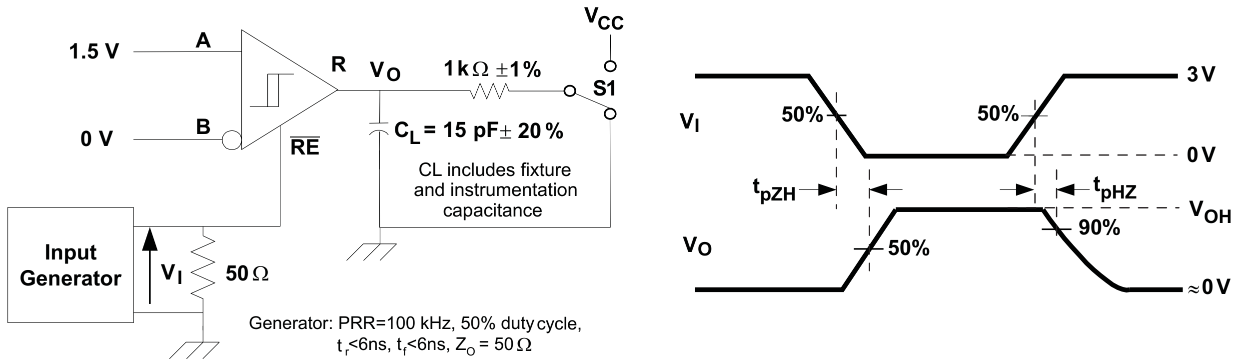



Figure 10. Receiver Enable Test Circuit and Waveforms, Data Output High

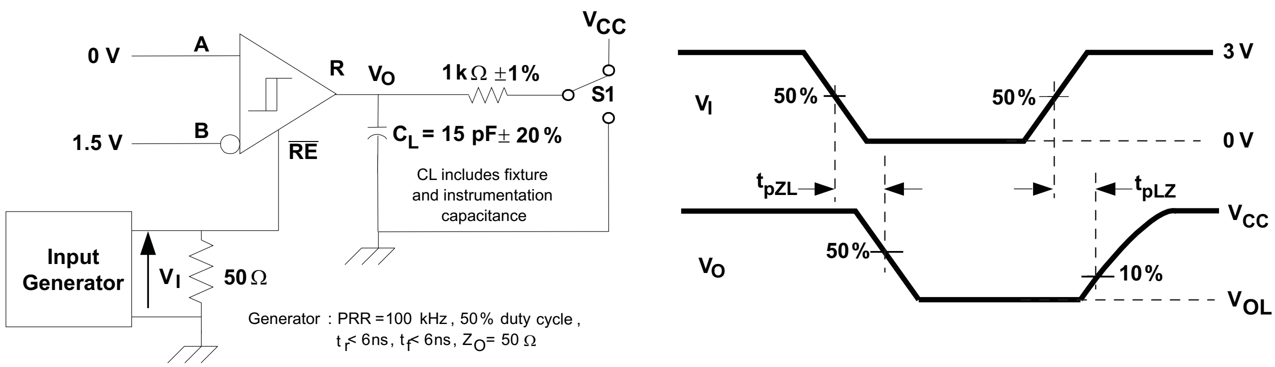



Figure 11. Receiver Enable Test Circuit and Waveforms, Data Output Low

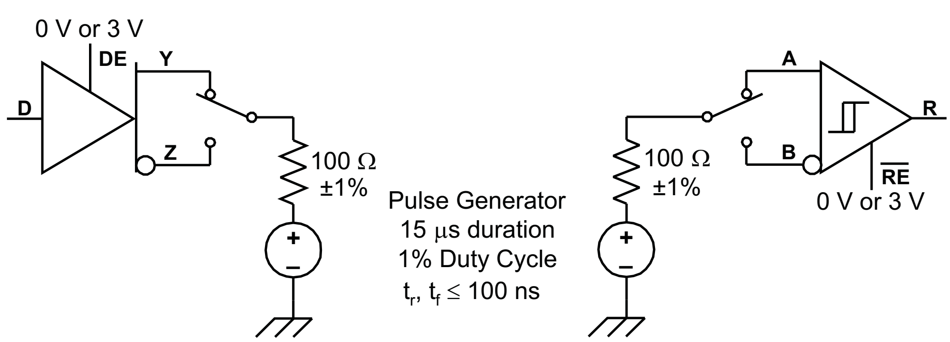



Figure 12. Transient Over-Voltage Test Circuit

## PARAMETER MEASUREMENT INFORMATION (continued)

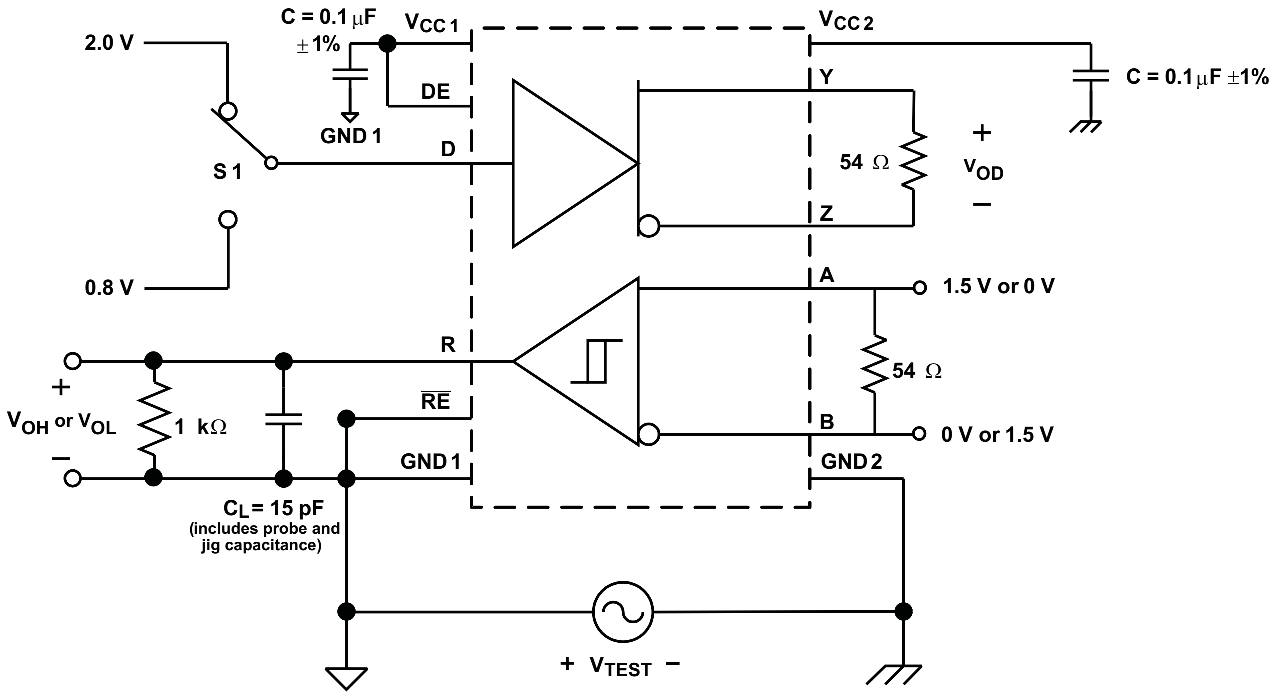



Figure 13. Common-Mode Transient Immunity Test Circuit

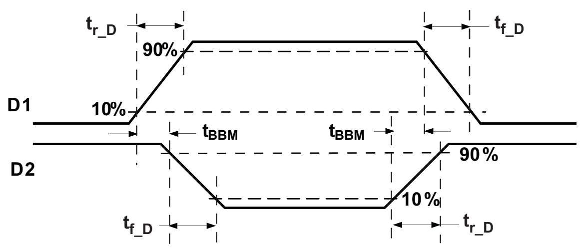



Figure 14. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs

# DEVICE INFORMATION

**Table 1. Driver Function Table(1)**

| INPUT | ENABLE | OUTPUTS | |
|---|---|---|---|
| (D) | (DE) | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | hi-Z | hi-Z |
| X | OPEN | hi-Z | hi-Z |
| OPEN | H | H | L |

(1) H = High Level, L= Low Level, X = Don't Care, hi-Z = High Impedance (Off)

**Table 2. Receiver Function Table(1)**

| DIFFERENTIAL INPUT $V_{ID} = (V_A – V_B)$ | ENABLE $(\overline{RE})$ | OUTPUT (R) |
|---|---|---|
| $–0.02\ V \leq V_{ID}$ | L | H |
| $–0.2\ V < V_{ID}\ –0.02\ V$ | L | ? |
| $V_{ID} \leq –0.2\ V$ | L | L |
| X | H | hi-Z |
| X | OPEN | hi-Z |
| Open circuit | L | H |
| Short Circuit | L | H |
| Idle (terminated) bus | L | H |

(1) H = High Level, L= Low Level, X = Don't Care, hi-Z = High Impedance (Off), ? = Indeterminate

## IEC INSULATION AND SAFETY RELATED SPECIFICATIONS FOR 16-DW PACKAGE

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| L(I01) | Minimum air gap (Clearance[(1)]) | Shortest terminal to terminal distance through air | 8.3 | | | mm |
| L(I02) | Minimum external tracking (Creepage[(1)]) | Shortest terminal to terminal distance across the package surface | 8.1 | | | mm |
| CTI | Tracking resistance(Comparative Tracking Index) | DIN IEC 60112 / VDE 0303 Part 1 | 400 | | | V |
| | Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.008 | | | mm |
| $R_{IO}$ | Isolation resistance | Input to output, $V_{IO}$ = 500 V, all pins on each side of the barrier tied together creating a two-terminal device | | $>10^{12}$ | | Ω |
| $C_{IO}$ | Barrier capacitance Input to output | $V_{IO}$ = 0.4 sin (2πft), f = 1 MHz | | 2 | | pF |
| $C_I$ | Input capacitance to ground | $V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, $V_{CC}$ = 5 V | | 2 | | pF |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications

## IEC 60664-1 RATINGS TABLE

| PARAMETER | TEST CONDITIONS | SPECIFICATION |
|---|---|---|
| Basic isolation group | Material group | II |
| Installation classification | Rated mains voltage ≤ 150 $V_{RMS}$ | I-IV |
| | Rated mains voltage ≤ 300 $V_{RMS}$ | I-III |
| | Rated mains voltage ≤ 400 $V_{RMS}$ | I-II |

## IEC 60747-5-2 INSULATION CHARACTERISTICS[(1)]

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SPECIFICATION | UNIT |
|---|---|---|---|---|
| $V_{IORM}$ | Maximum working insulation voltage | | 566 | Vpeak |
| $V_{PR}$ | Input to output test voltage | Method b1, $V_{PR} = V_{IORM}$ × 1.875, 100% Production test with t = 1 s, Partial discharge < 5 pC | 1062 | Vpeak |
| | | Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ × 1.6, t = 10 s, Partial discharge < 5pC | 906 | |
| | | After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC | 680 | |
| $V_{IOTM}$ | Transient overvoltage | t = 60 s (Qualification) t = 1 s (100% Production) | 4242 | Vpeak |
| $V_{IOSM}$ | Maximum surge voltage | Tested per IEC 60065 (Qualification Test) | 4242 | $V_{peak}$ |
| $R_S$ | Insulation resistance | $V_{IO}$ = 500 V at $T_S$ | $> 10^9$ | Ω |
| | Pollution degree | | 2 | |

(1) Climatic Classification 40/125/21

## REGULATORY INFORMATION

| VDE | UL |
|---|---|
| Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2) | Recognized under 1577 Component Recognition Program |
| Basic Insulation<br>Maximum Transient Overvoltage, 4242 $V_{PK}$<br>Maximum Surge Voltage, 4242 $V_{PK}$<br>Maximum Working Voltage, 566 $V_{PK}$ | Single / Basic Isolation Voltage, 2500 $V_{RMS}$ (1) |
| File Number: 40016131 (Approval Pending) | File Number: E181974 (Approval Pending) |

(1) Production tested ≥ 3000 $V_{RMS}$ for 1 second in accordance with UL 1577.

## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply. Without current limiting, sufficient power is dissipated to overheat the die; and, damage the isolation barrier—potentially leading to secondary system failures.

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | DW-16 | $\theta_{JA}$ = 80.5°C/W, $V_I$ = 3.6V, $T_J$ = 170°C, $T_A$ = 25°C | | | 500 | mA |
| $T_S$ | Maximum case temperature | | | | | 150 | °C |

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on the High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

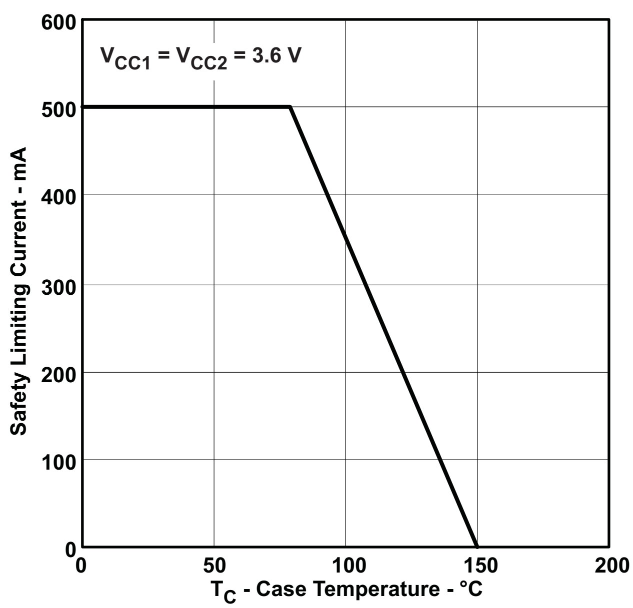


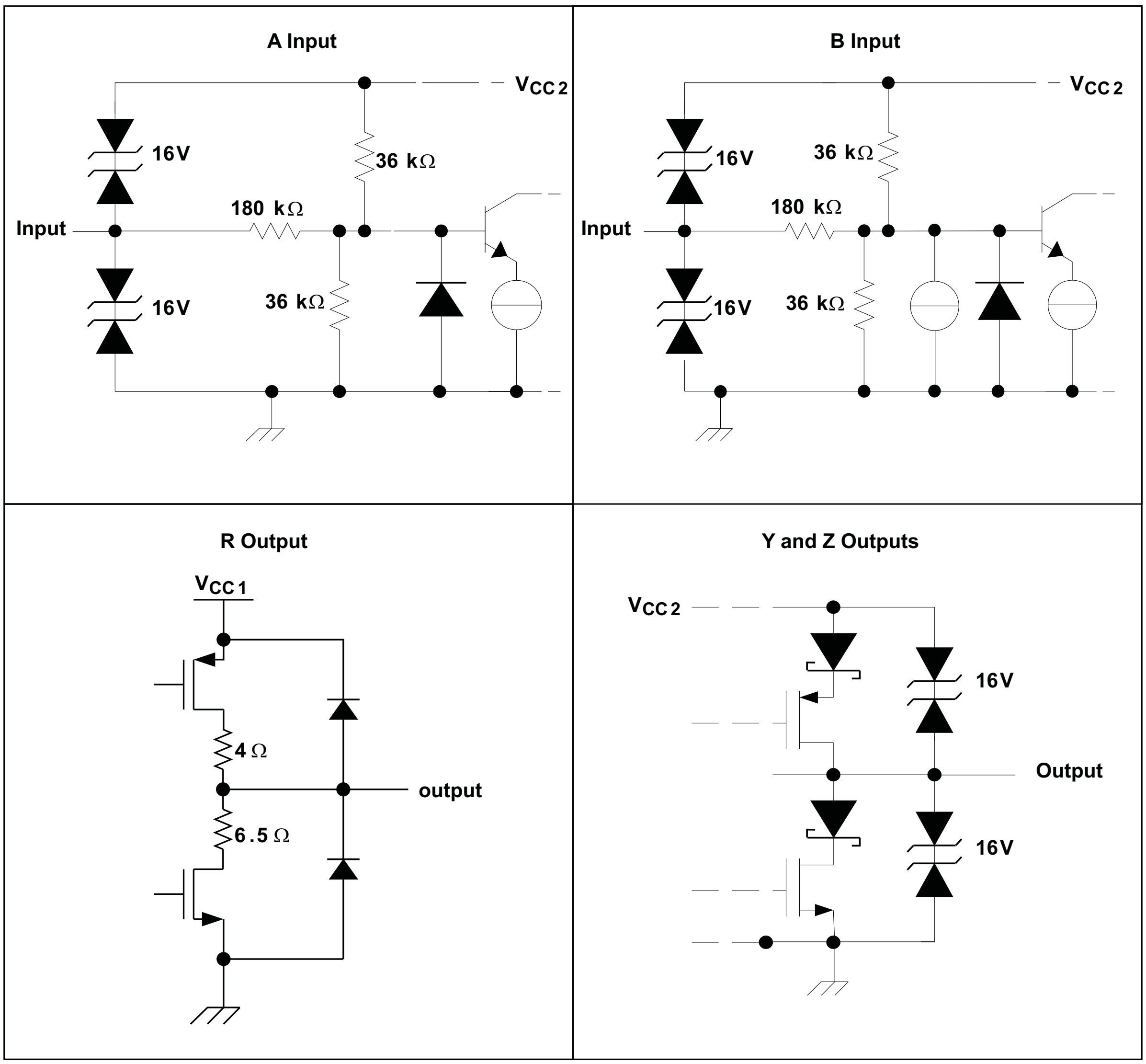

**Figure 15. DW-16 $\theta_{JC}$ Thermal Derating Curve per IEC 60747-5-2**

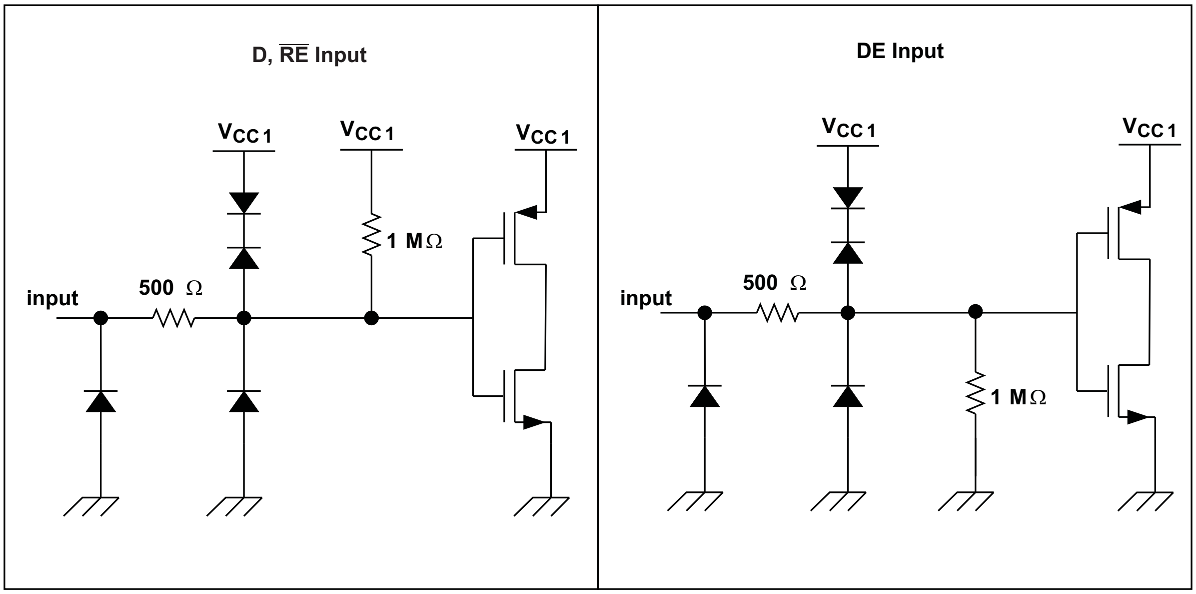
## THERMAL INFORMATION

| THERMAL METRIC(1) | | ISO35T DW 16 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 80.5 | °C/W |
| $\theta_{JC(TOP)}$ | Junction-to-case(top) thermal resistance | 43.8 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 49.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 13.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 41.4 | |
| $\theta_{JC(BOTTOM)}$ | Junction-to-case(bottom) thermal resistance | n/a | |
| $P_D$ (2) | $V_{CC1} = V_{CC2}$ = 3.6V, $T_J$ = 150°C, $R_L$ = 54Ω, $C_L$ = 50pF (Driver), $C_L$ = 15pF (Receiver), Input a 0.5 MHz 50% duty cycle square wave to Driver and Receiver | 373 | mW |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) $P_D$ = Maximum device power dissipation

## EQUIVALENT CIRCUIT SCHEMATICS




D, RE Input
VCC 1
VCC 1
VCC 1
1 MΩ
500 Ω
input
DE Input
VCC 1
VCC 1
500 Ω
input
1 MΩ

## TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
DATA RATE WITH NO LOAD

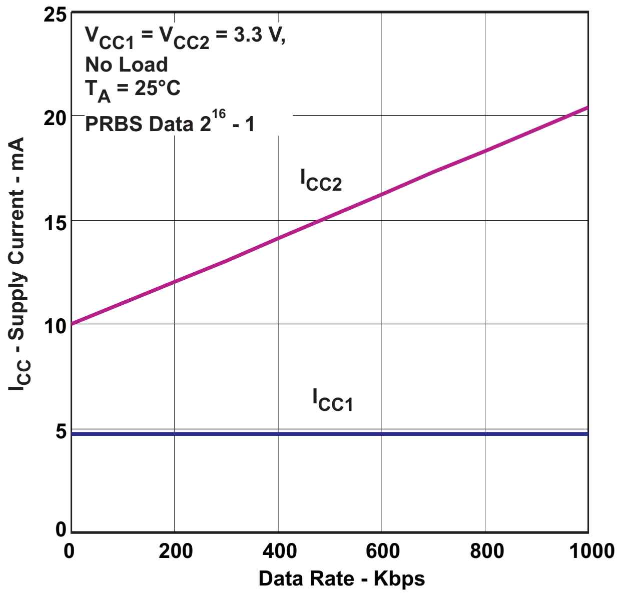



Figure 16.

SUPPLY CURRENT
vs
DATA RATE WITH LOAD

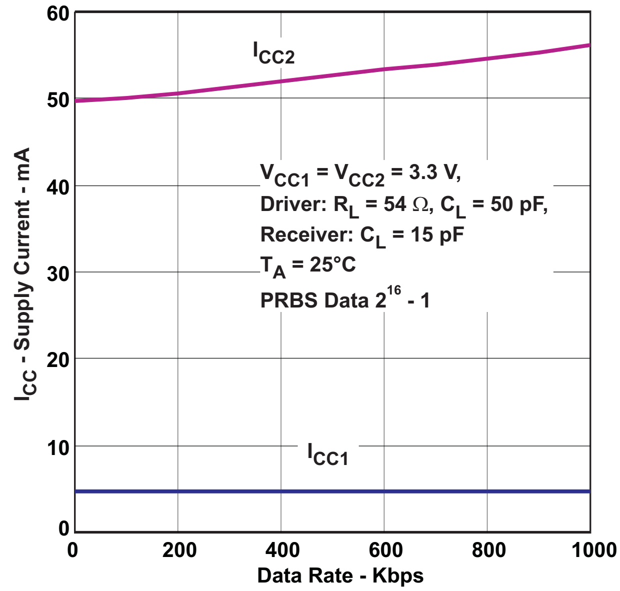



Figure 17.

DRIVER PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

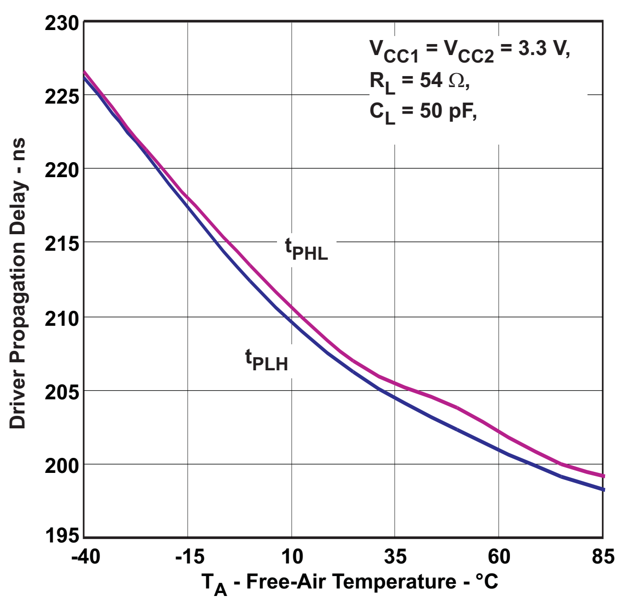



Figure 18.

RECEIVER PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

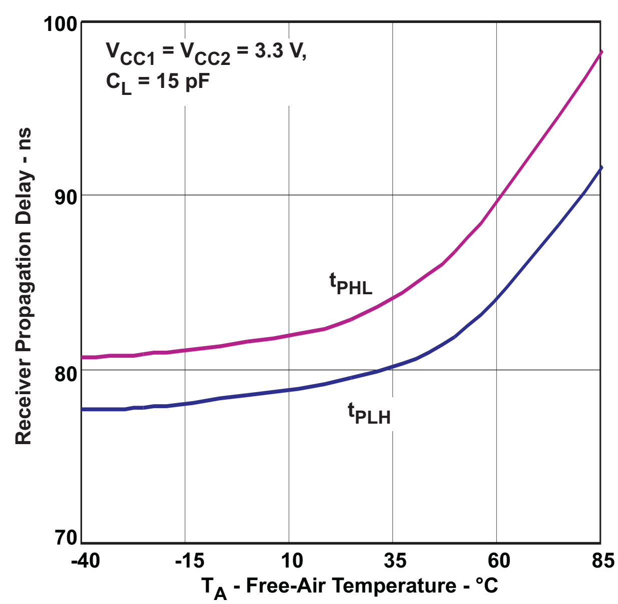



Figure 19.

## TYPICAL CHARACTERISTICS (continued)

**DRIVER RISE, FALL TIME vs FREE-AIR TEMPERATURE**

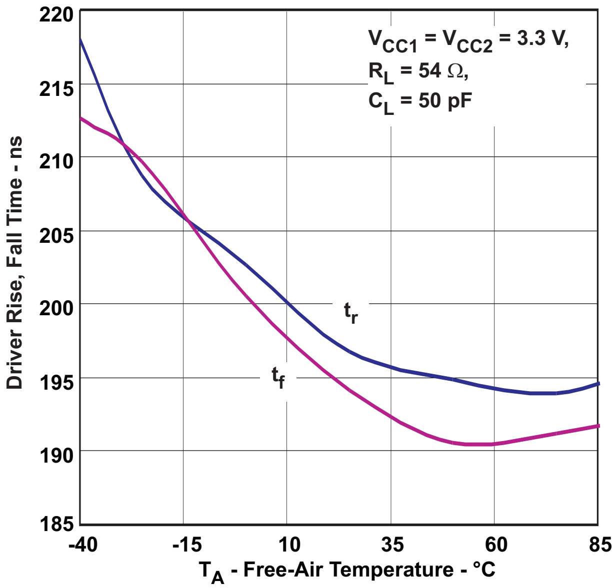



Figure 20.

**RECEIVER RISE, FALL TIME vs FREE-AIR TEMPERATURE**

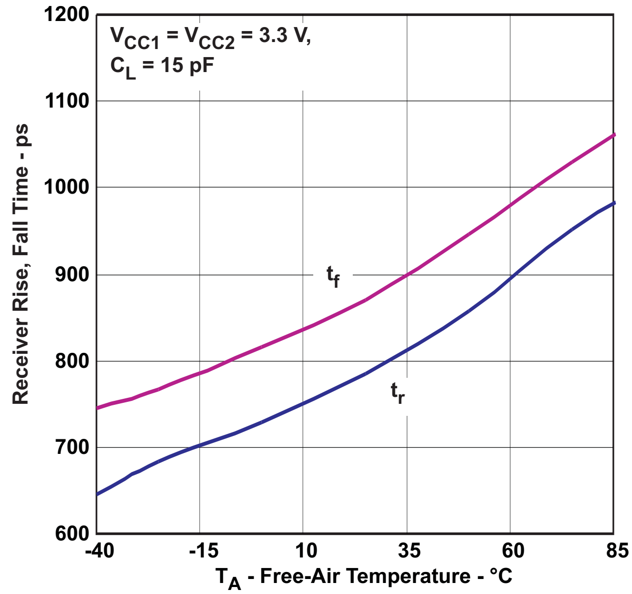



Figure 21.

**DIFFERENTIAL OUTPUT VOLTAGE vs LOAD CURRENT**

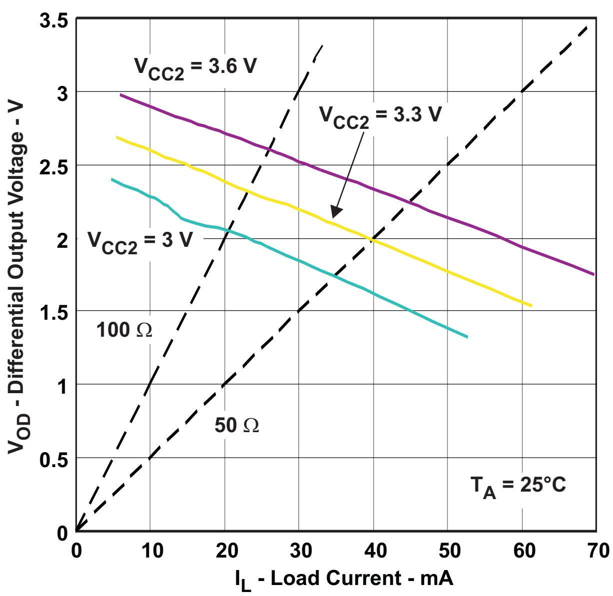



Figure 22.

**RECEIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

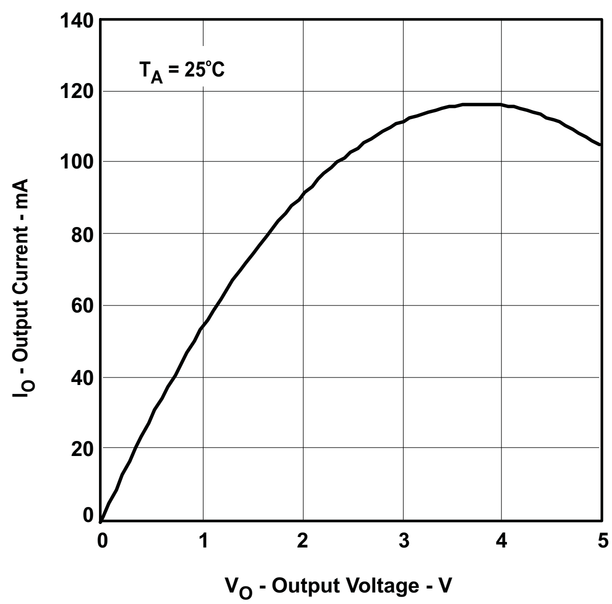



Figure 23.

## TYPICAL CHARACTERISTICS (continued)

**RECEIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

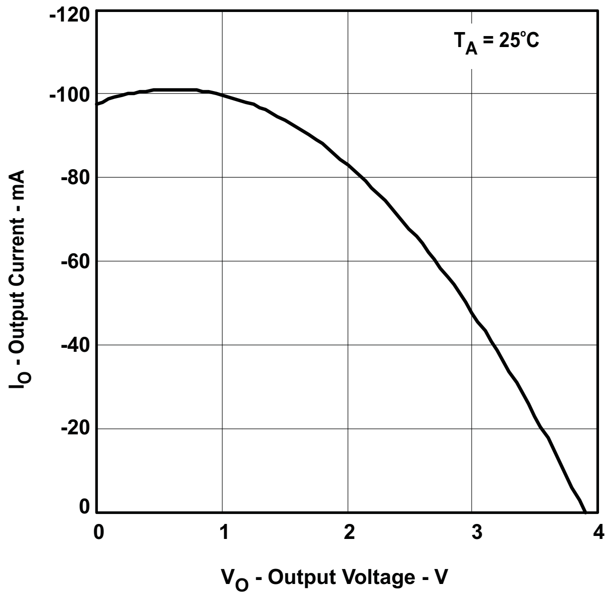



Figure 24.

**BUS INPUT CURRENT vs INPUT VOLTAGE**

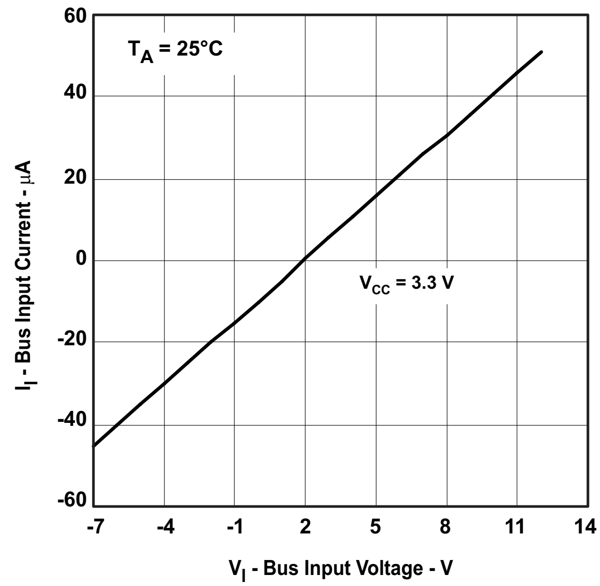



Figure 25.

## APPLICATION INFORMATION

### REFERENCE DESIGN

ISO35T Reference design (*sluu470*) and miniature evaluation boards are available to provide a complete isolated data and power solution.

### TRANSIENT VOLTAGES

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO35T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can easily exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but very high voltage transients.

Figure 26 models the ISO35T bus IO connected to a noise generator. $C_{IN}$ and $R_{IN}$ is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, $C_{ISO}$ and $R_{ISO}$ is the capacitance and resistance between GND1 and GND2 of ISO35T plus those of any other insulation (transformer, etc.), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is $v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}}$ and will always be less than 16 V from $V_N$.

If ISO35T is tested as a stand-alone device, $R_{IN} = 6 \times 10^4 \Omega$, $C_{IN} = 16 \times 10^{-12}$ F, $R_{ISO} = 10^9 \Omega$ and $C_{ISO} = 10^{-12}$ F.

Note from Figure 26 that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency,

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4}$$

or essentially all noise appears across the barrier.

At very high frequency,

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94$$

and 94% of $V_N$ appears across the barrier. As long as $R_{ISO}$ is greater than $R_{IN}$ and $C_{ISO}$ is less than $C_{IN}$, most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

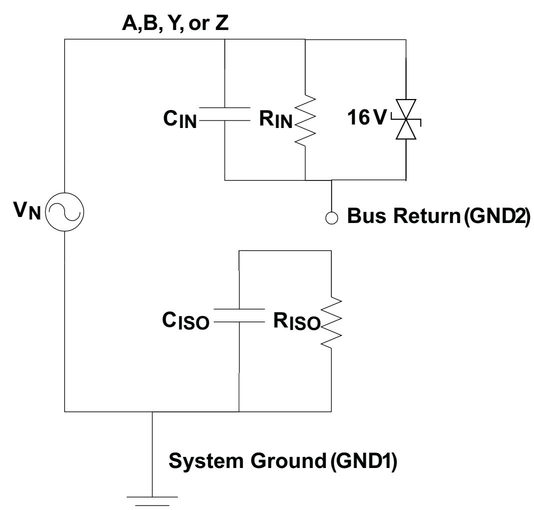



**Figure 26. Noise Model**

## REVISION HISTORY

| Changes from Original (November 2010) to Revision A | Page |
|---|---|
| • Changed the data sheet From: Product Preview To: Production data | 1 |

| Changes from Revision A (March 2011) to Revision B | Page |
|---|---|
| • Changed pin 16 From: $V_{CC1}$ To: $V_{CC2}$ in the DW Package drawing | 1 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| ISO35TDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | Call TI | Level-3-260C-168 HR | |
| ISO35TDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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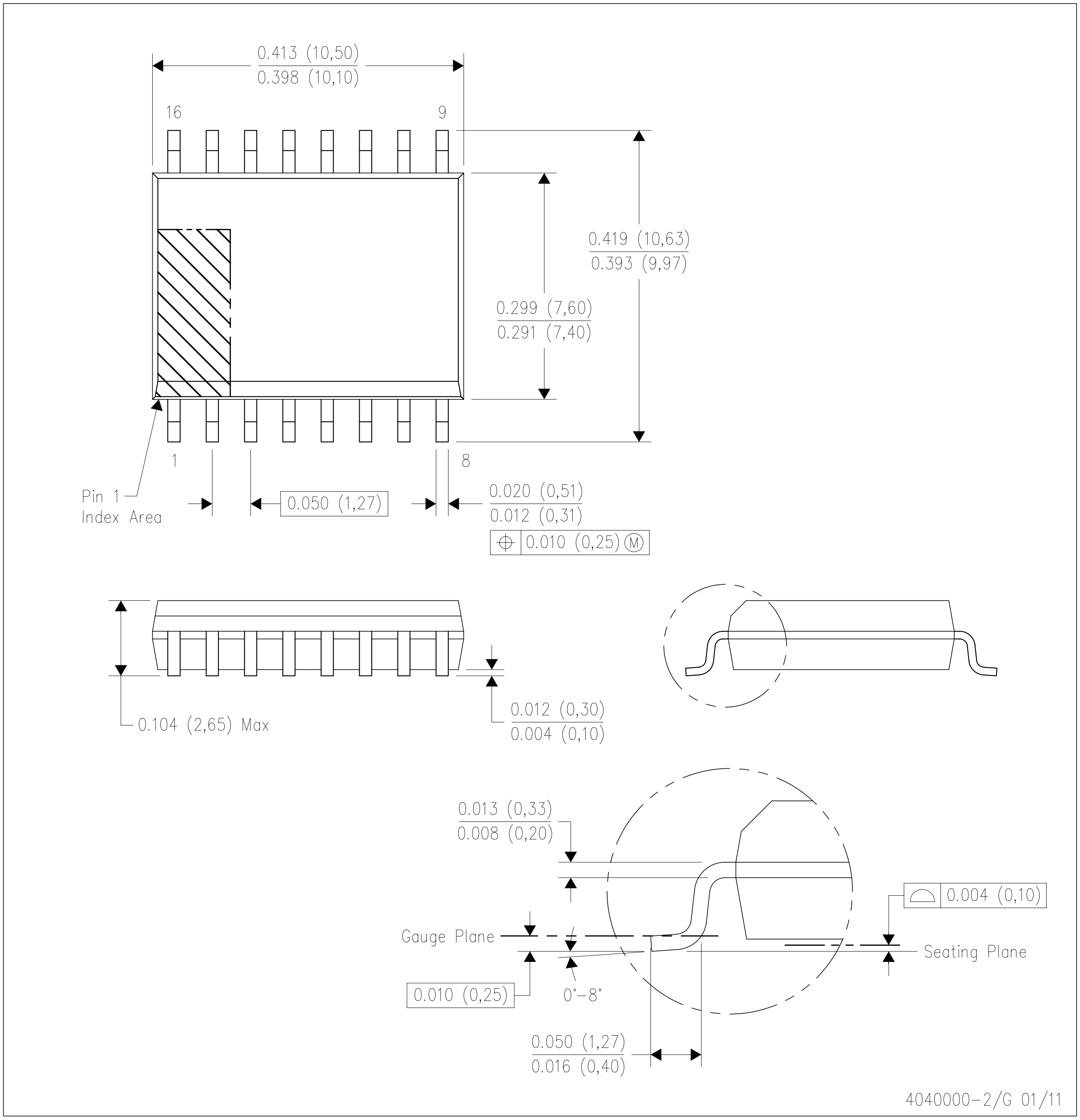
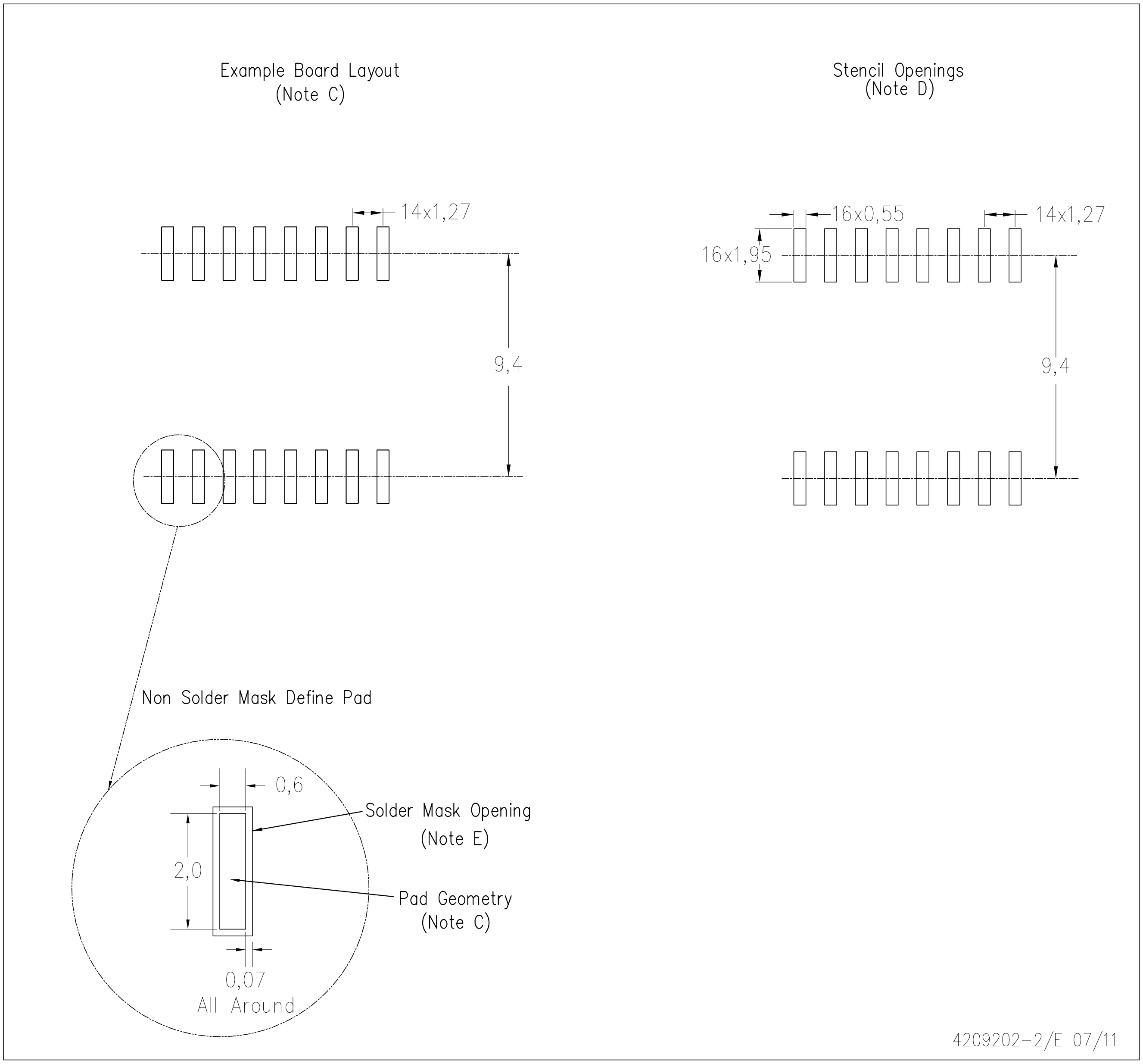
DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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